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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,629	12/28/2000	Yuanlong Wang	00CXT0785N	7116

36122 7590 08/24/2004

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,629	WANG ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aybay (US Patent 6,185,221) in view of Olnowich et al. (US Patent 5,920,704).

As per claim 1, Aybay discloses communication circuitry comprising:

- parallel channels (col.2, lines 1-5) configured to transfer; (col.8, lines 5-21), (col.5, lines 66-67), (col.6, lines 8-11)
- processing circuitry configured to exchange the communications between communication links (col.10, lines 56-64) and the parallel channels; and (col.3, lines 29-36), (col.7, lines 38-45)
- crossbar (fig.5, 60) integrated circuits configured to receive the communications over the parallel channels, and transfer the switched communications to the parallel channels. (col.8, lines 5-21), (col.5, lines 66-67), (col.6, lines 8-11)

Aybay discloses all the limitations as above except communications in parallel with a clock signal. However, Onowich discloses one signal line in the interface to each input and output

port of an asynchronous switch for the purpose of transmitting a clock pulse with each data character sent to the switch. Transmitting individual clock lines to/from each input/output port implements the relatching function as individual islands of logic. (col.3 lines 45-67)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Onowich's teaching into Aybay's system so as to improve an asynchronous switching by enabling it to reshape data pulses and eliminate skewing problems as data is transmitted through the switch. (col.3, lines 37-40)

As per claim 11, Aybay discloses the method operating communication circuitry, the method comprising:

- exchanging communications between communication links and processing circuitry; (col.7, lines 38-45)
- exchanging the communications between the processing circuitry and parallel channels; (col.2, lines 1-5), (col.8, lines 5-21)
- transferring the communications in parallel over the parallel channels; (col.3, lines 29-36)
- receiving the communications from the parallel channels into crossbar integrated circuits; (col.6, lines 8-11)
- switching the communications in the crossbar integrated circuits, and (col.8, lines 5-21)

- transferring the switched communications from the crossbar integrated circuits to the parallel channels. (fig.5), (col.7, lines 14-18)

Aybay discloses all the limitations as above except communications in parallel with a clock signal. However, Onowich discloses one signal line in the interface to each input and output port of an asynchronous switch for the purpose of transmitting a clock pulse with each data character sent to the switch. Transmitting individual clock lines to/from each input/output port implements the relatching function as individual islands of logic. (col.3 lines 45-67)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Onowich's teaching into Aybay's system so as to improve an asynchronous switching by enabling it to reshape data pulses and eliminate skewing problems as data is transmitted through the switch. (col.3, lines 37-40)

As per claims 2,12, Olnowich discloses wherein the parallel channels are each comprised of parallel differential signal pairs wherein one of the differential signal pairs is for the clock signal. (col.3, lines 61-63)

As per claim 3, Aybay discloses the communication links comprise serial channels. (col.1,lines 35-40)

As per claims 4, 14, Aybay discloses the communications comprise data packets. (fig.6, 150), (col.6, lines 42-45)

As per claims 5, 15, Aybay discloses the communications comprise fixed-length data packets. (col.7, lines 57-64)

As per claims 7, 17, Aybay discloses the processing circuitry is comprised of virtual output queues that store the communications prior to switching and that are associated with egress ports. (col.10, lines 53-64), (col.8, lines 41-57)

As per claims 8, 18, Aybay discloses the processing circuitry is comprised of virtual output queues that store the communications prior to switching and wherein each virtual output queue (fig.8, 42) is comprised of sub-queues (fig.8, 132) that are each associated with a different priority. (col.8, lines 50-60)

As per claims 9, 19, Aybay discloses the processing circuitry is comprised of a multi-cast virtual output queue that stores the communications prior to switching for multi-cast output. (col.2, lines 1-5), (col.1, lines 57-67)

As per claims 10, 20, Aybay discloses the parallel channels include multiplexers (fig.8, 130) to perform bit slicing through the crossbar integrated circuits. (col.10, lines 34-36)

As per claim 13, Aybay discloses exchanging the communications between the communication links and the processing circuitry comprises exchanging the communications between serial channels and the processing circuitry. (col.1, lines 26-40)

Response to Amendment

2. Applicant's argument filed on 5/13/04 have been fully considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Yamamoto does not discloses parallel channels configured to transfer communications in parallel with a clock signal. However, Olnowich discloses a parallel system; data are transferred in parallel; each signal line (channel) in the interface to each input and output port of switch for the purpose of transmitting a clock pulse with each data character sent to the switch. (col.3, lines 4-67). Thus, the prior art teaches the invention as claimed, the claims do not distinguish over the prior art as applied.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

August 22, 2004

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100